

FIG. 1(a)

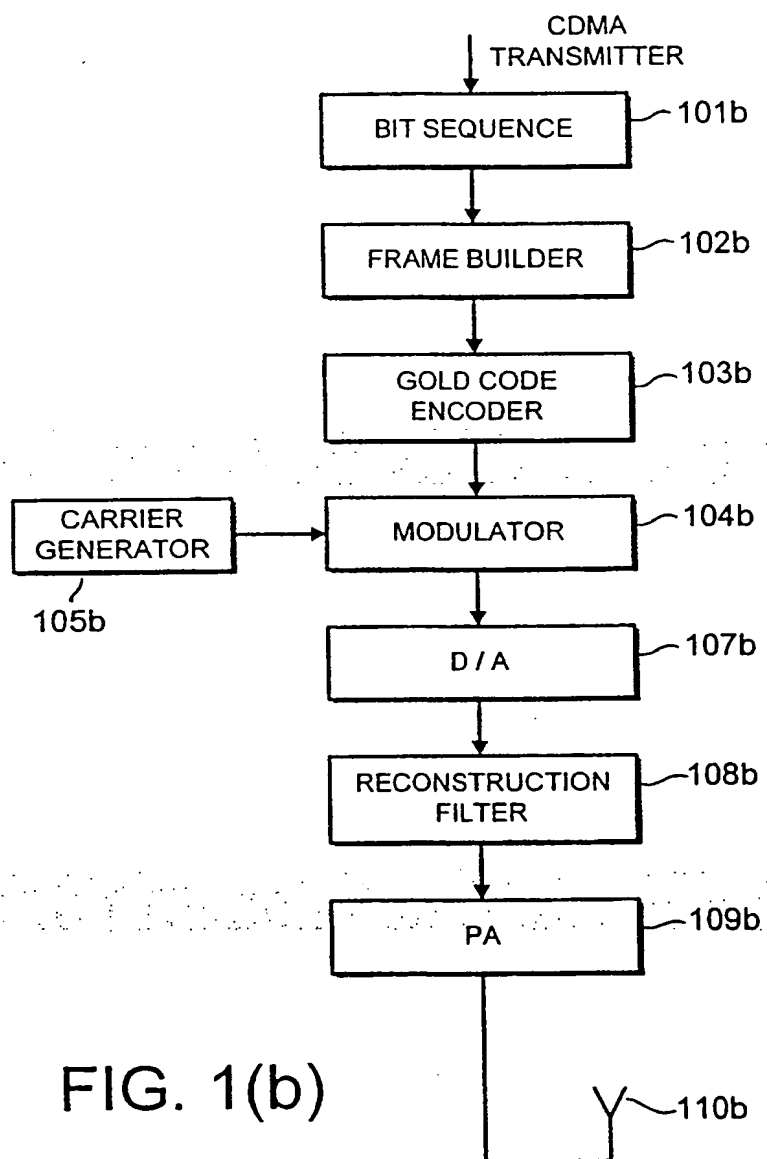


FIG. 1(b)

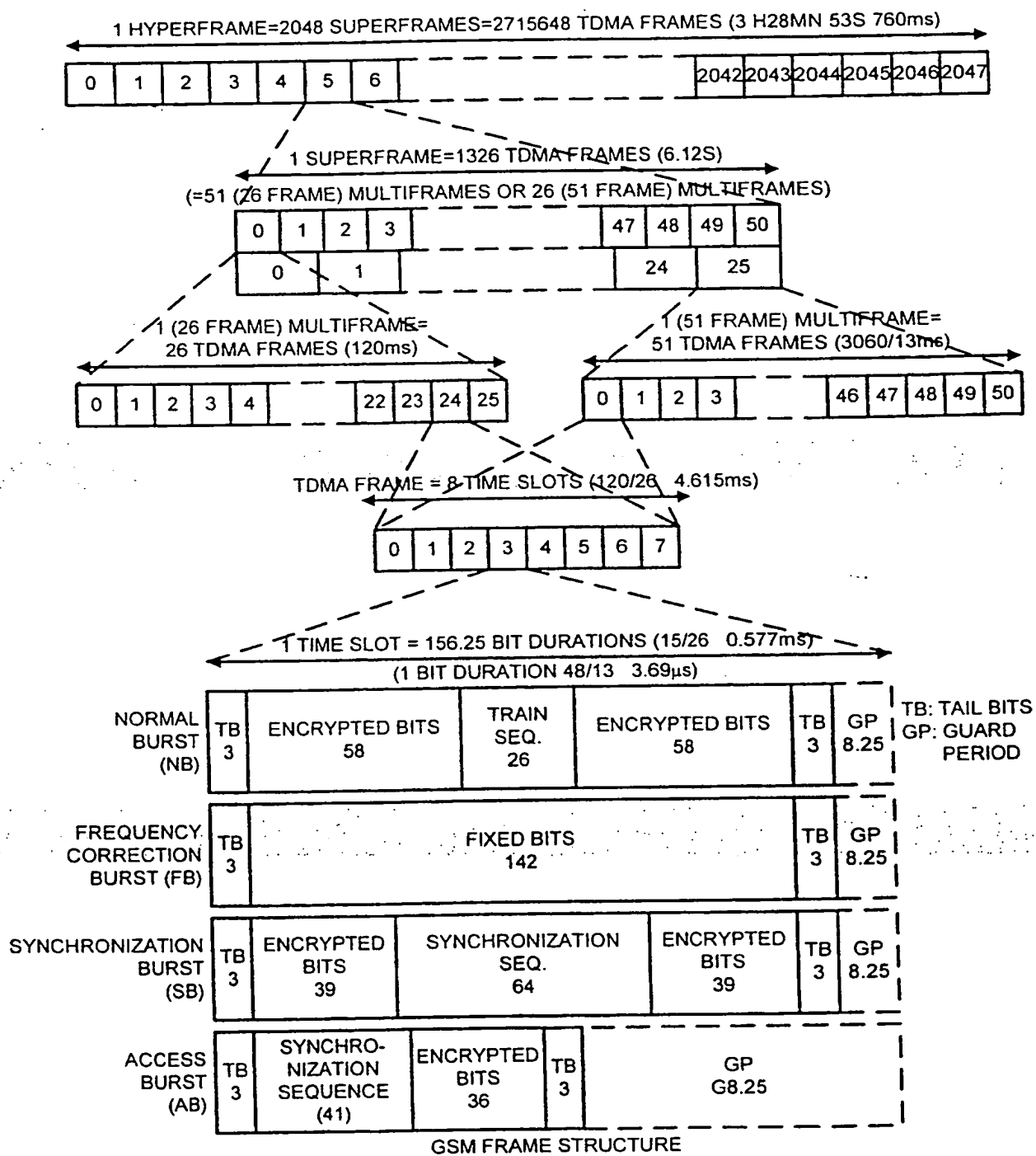


FIG. 1(c)

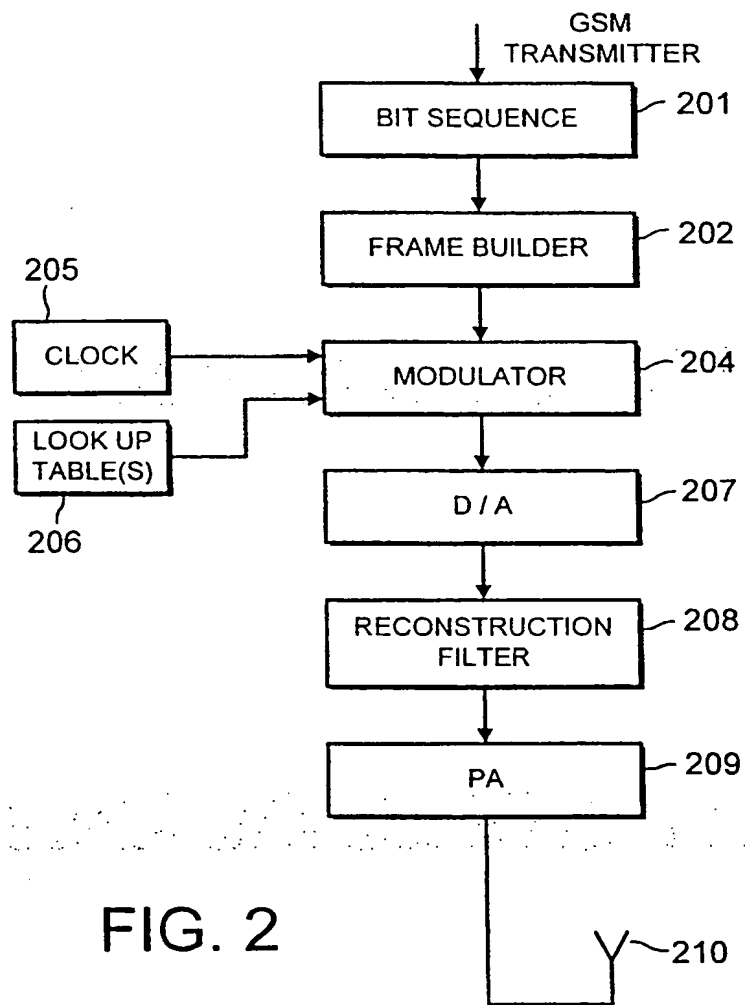


FIG. 2

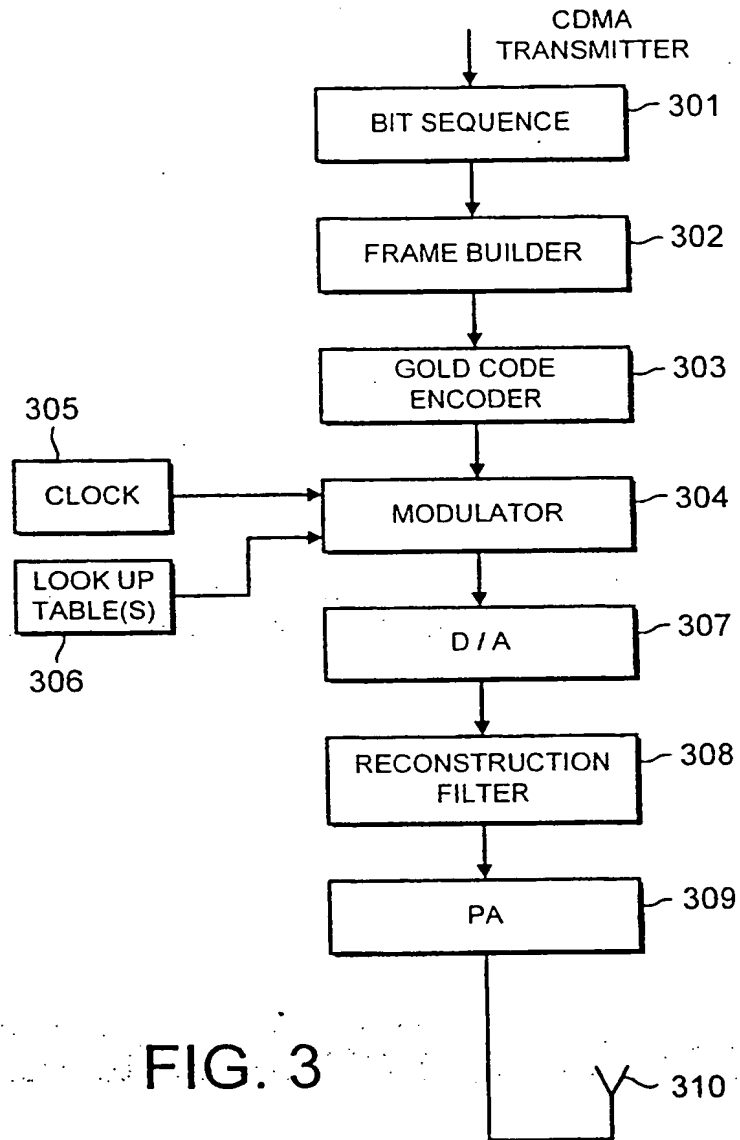


FIG. 3

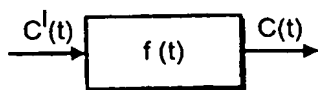
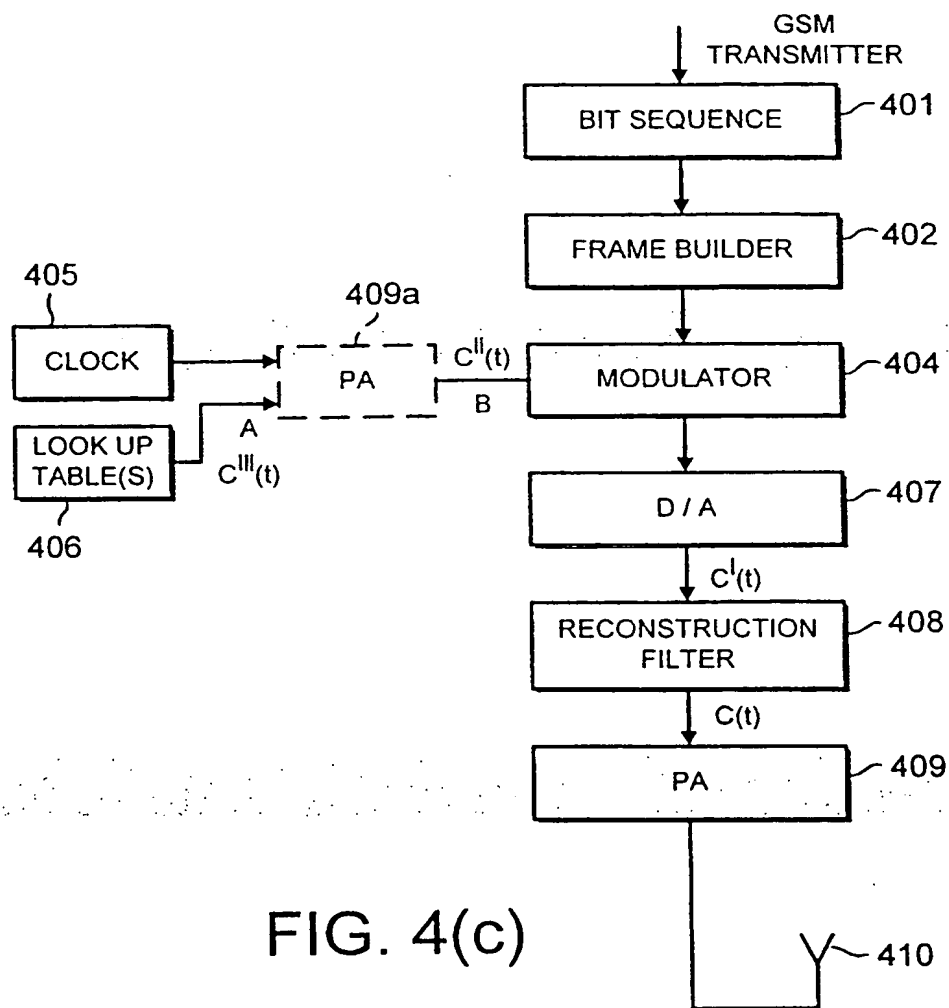


FIG. 4(a)



FIG. 4(b)



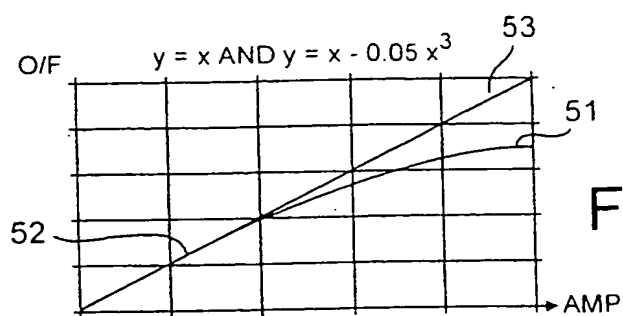


FIG. 5(a)

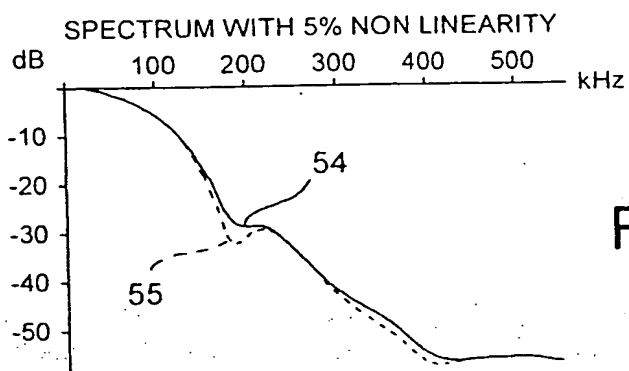


FIG. 5(b)

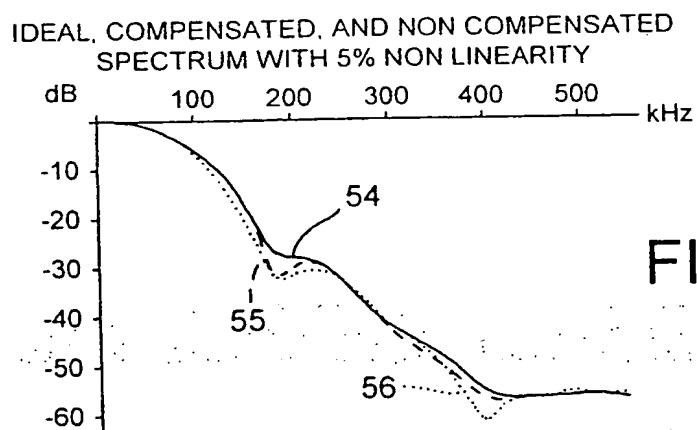


FIG. 5(c)

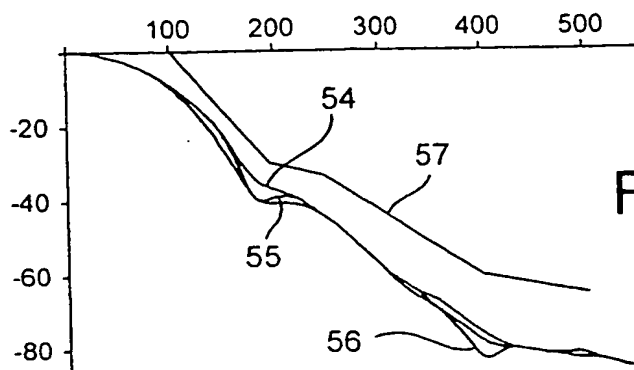


FIG. 5(d)

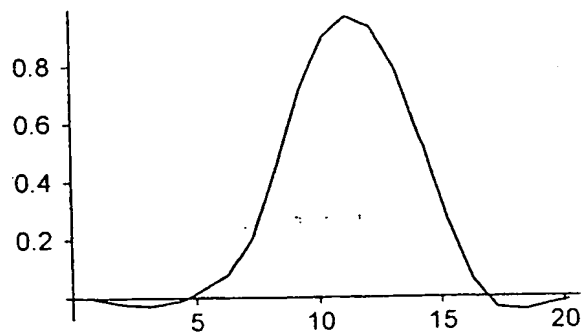


FIG.6(a)

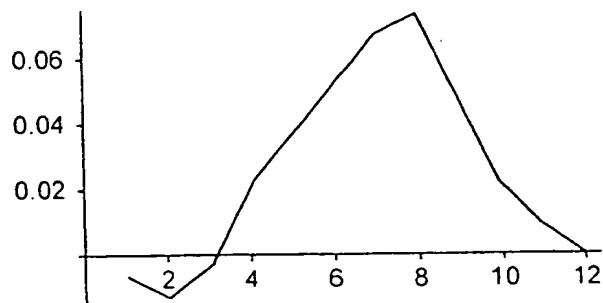


FIG.6(b)

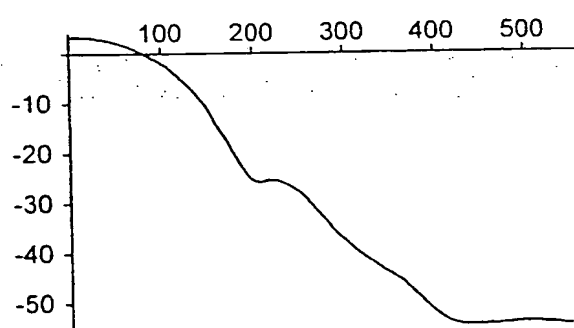


FIG.6(c)

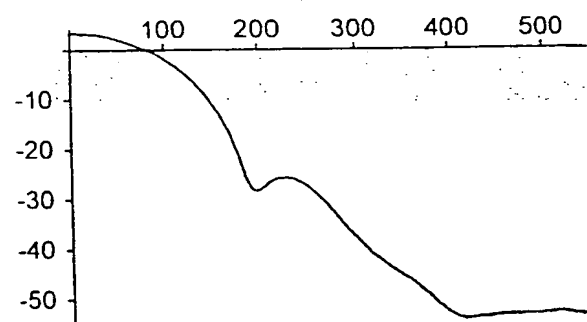


FIG.6(d)

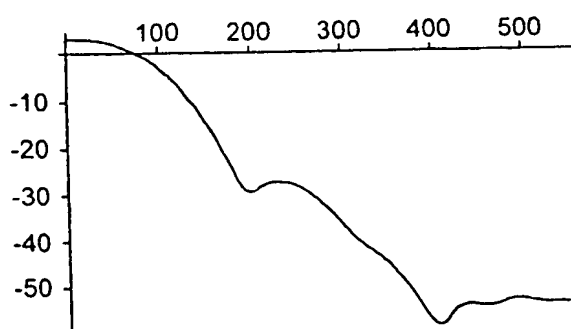


FIG.6(e)

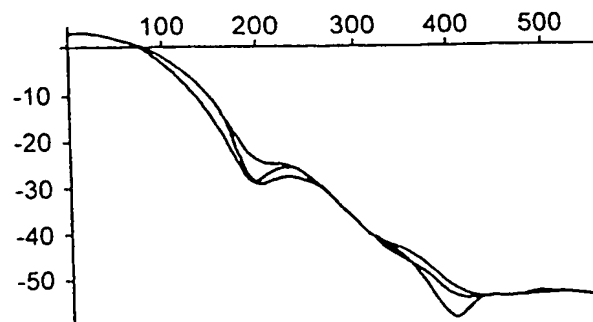


FIG.6(f)



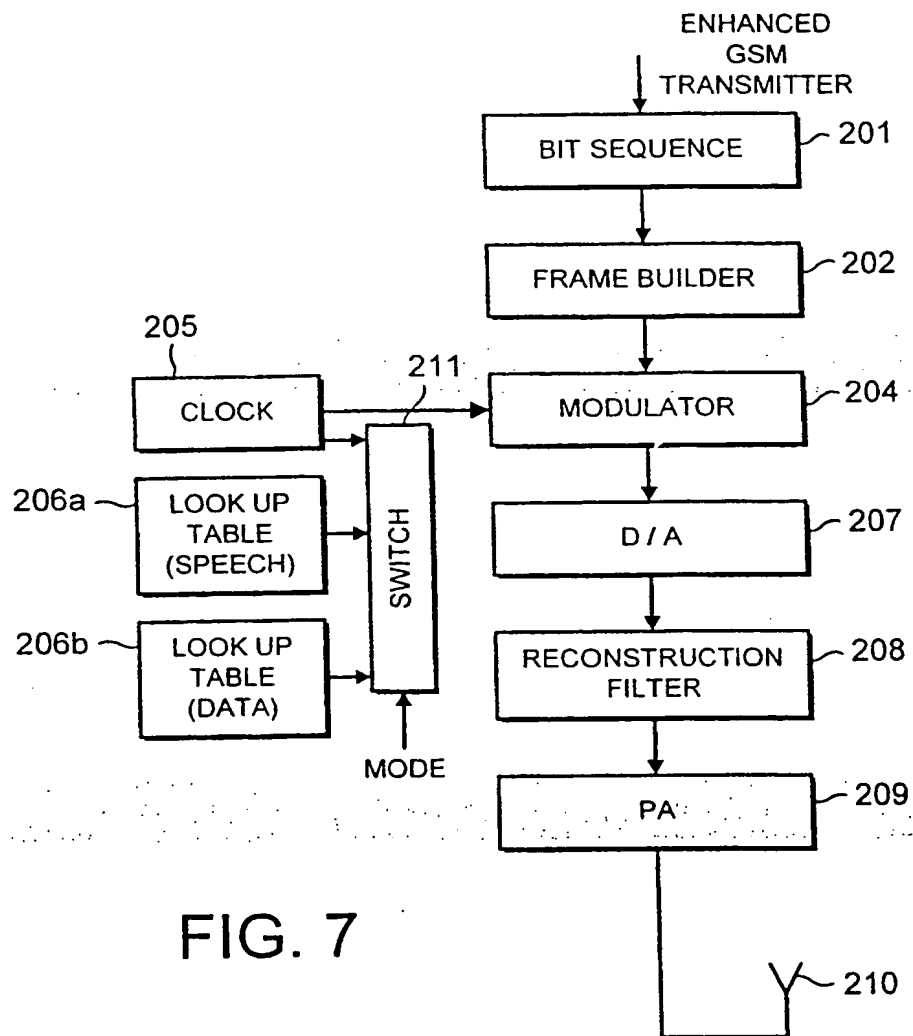
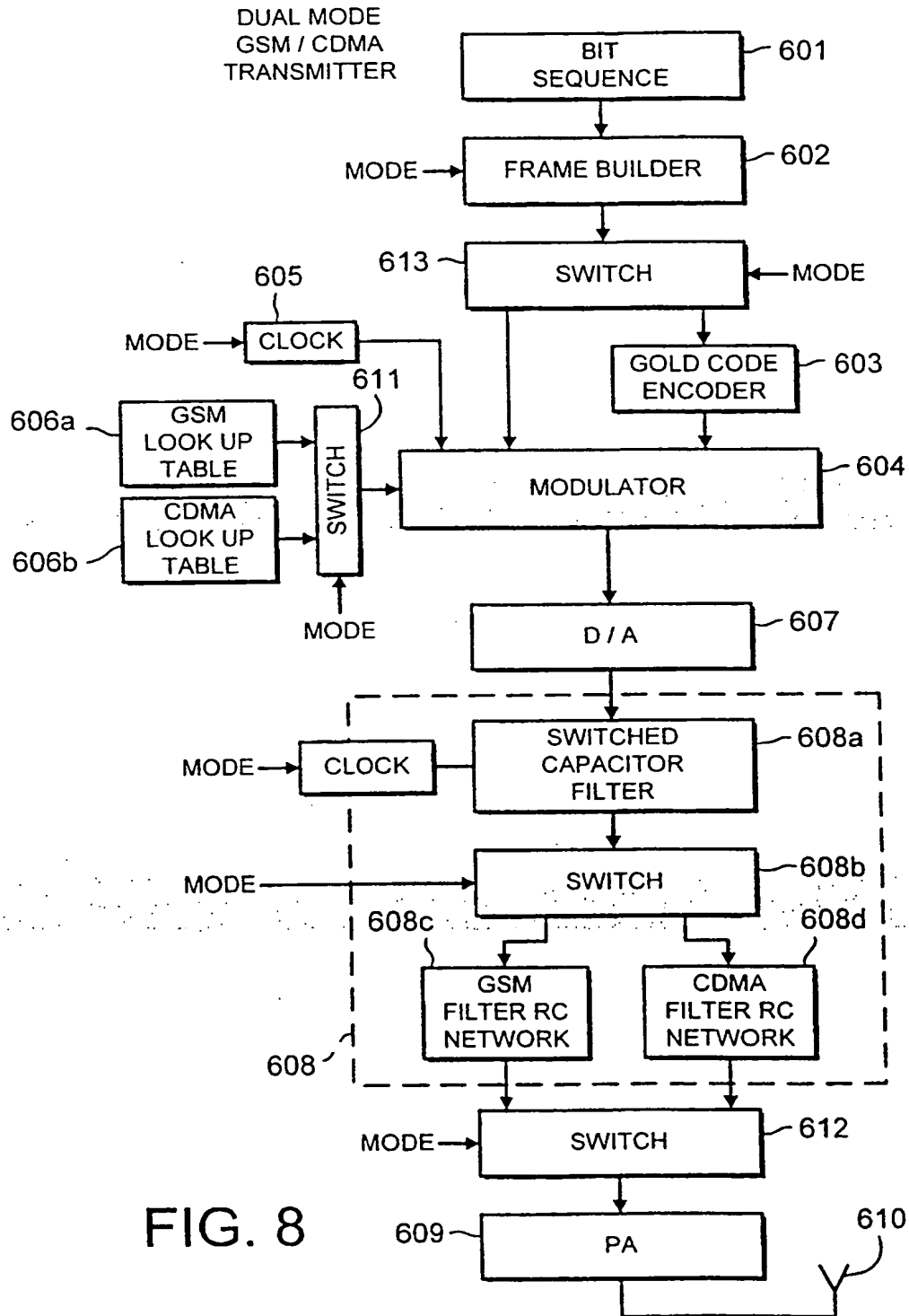


FIG. 7



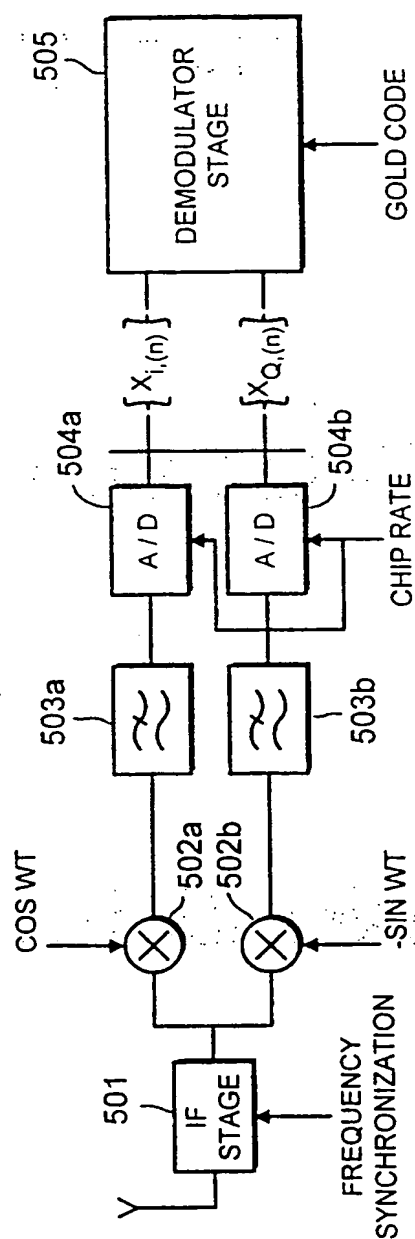
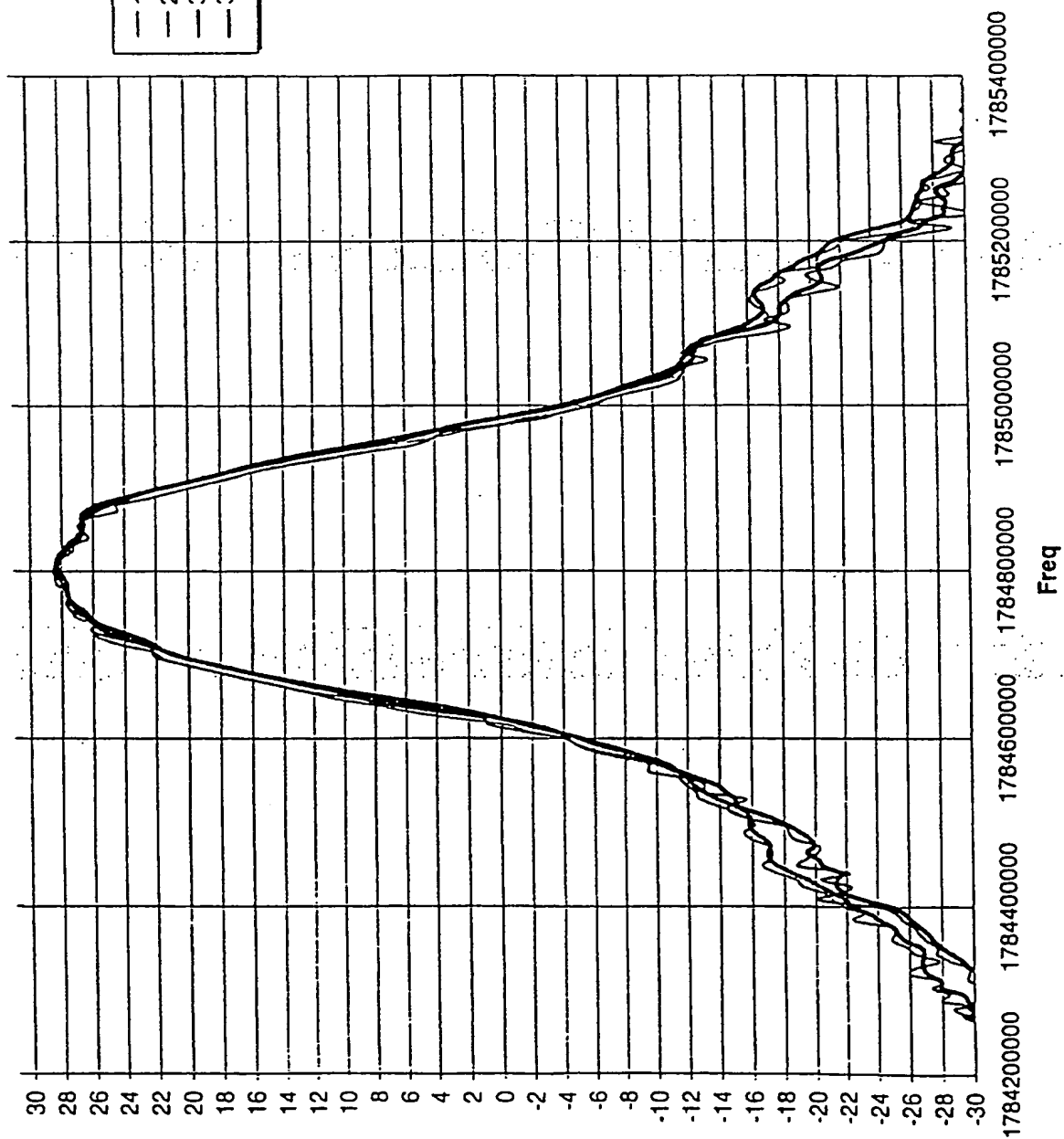


FIG. 9

FIG.10(a)



PHASE ERROR rms max

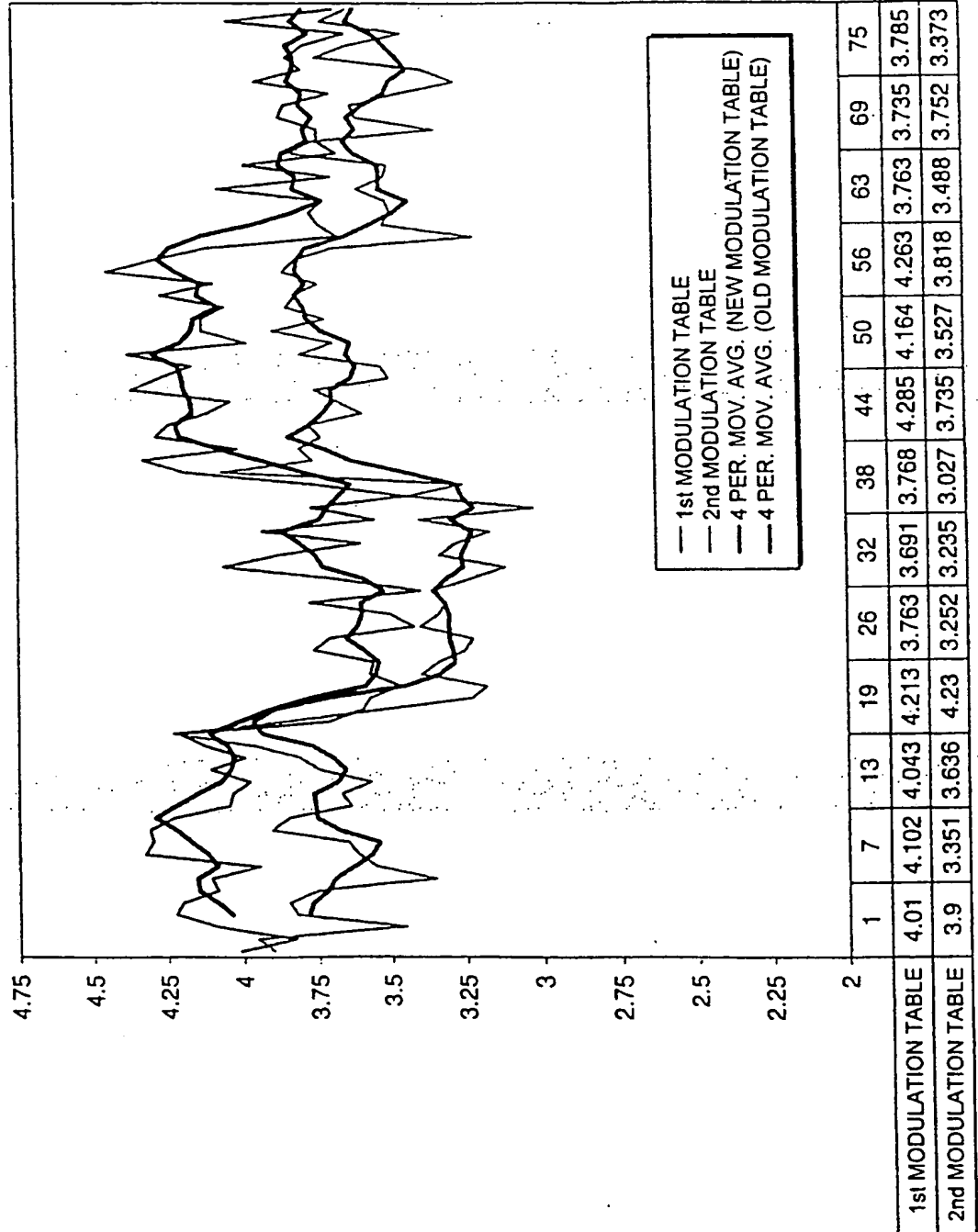


FIG.10(b)